Customer No.: 31561
Application No.: 10/605,323
Docket No.: 10680-US-PA

REMARKS

Present Status of the Application

The drawings are objected to because of informalities. The Office Action rejected claims 1 and 5-8 under 35 U.S.C. 102(b), as being anticipated by Sakamoto et al. (U.S. 2003/0030768). The Office Action also rejected claims 2-4 and 9-14 under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al. in view of Matsueda (U.S. 5,173,792). Applicants have amended drawings to overcome the objection and have amended claims 1, 8 and 10 and cancel claims 2-3 and 9 to improve clarity. After entry of the foregoing amendments, claims 1, 4-8 and 10-14 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Summary of Applicant's Invention

The Applicant's invention is directed to a pixel structure and a fabricating method thereof. In the present invention, the common line 218, the gate line 202 and the gate electrode 206 are formed together over the substrate. That is, the common line 218, the gate line 202 and the gate electrode 206 belong to a Metal 1 layer (as shown in Figs. 2 and 3 and paragraph [0022]). After the gate insulating layer is formed over the substrate, the data line 204, the conducting layer 250 and the source/drain electrodes 210a/210b are together formed over the substrate. That is, the data line 204, the conducting layer 250 and the source/drain electrodes 210a/210b belong to a Metal 2 layer (as shown in Figs. 2 and 3 and paragraph [0026]). More specifically, the conducting layer 250 comprises a coupling portion 220 and a connecting portion 240, wherein the coupling portion 220 is positioned above the common line 218 and the connecting portion 240 connects the

coupling portion 220 and the drain electrode 210b. Also, the connecting portion 240 further includes a multi-channel portion 224 having several channels (224a, 224b and 224c). Moreover, after the passivation layer 211 and the planarization layer 213 are formed over the substrate, the contact window 228 is formed in the passivation layer 211 and the planarization layer 213 and over the multi-channel portion 224 of the connecting portion 240 to expose at least one of the channels. Finally, a pixel electrode 212 formed over the substrate and is electrically connected to the exposed channel in the contact window 228 so that the pixel electrode 212 is also electrically connected to the drain electrode 210b through the connecting portion 240 of the conductive layer 250.

Discussion of objections

According to the Office Action, the drawings were objected to because Figs. 2-4, which should have meant for the present invention and have been examined accordingly, are presently stated as "PRIOR ART". In response thereto, Applicants have amended Figs. 2-4 by deleting phrases "PRIOR ART".

Discussion of Office Action Rejections

The Office Action rejected claims 1 and 5-8 under 35 U.S.C. 102(b), as being anticipated by Sakamoto et al. (U.S. 2003/0030768) asserted that the cited art disclosed all the claimed features of the present invention.

Applicants respectfully traverse this rejection but have amended claims 1 and 8 to clearly define the structure and the method according to the present invention. As amended, claims 1 and 8 recite, respectively:

Claim 1. A pixel structure, comprising:

a gate line, located on a substrate;

.....

a conducting layer, located on said gate insulating layer, said conducting layer including a coupling portion and a connecting portion, said coupling portion being above said common line for a top electrode of said pixel storage capacitor, said connecting portion comprising a first portion, a second portion and the third portion, wherein said first portion is coupled to said coupling portion, said second portion is connected to said switching device and **said third portion located between said first portion and said second portion possesses a plurality of channels**;

a passivation layer, covering said data line, said switching device, and said conducting layer;

a contact window, disposed in said passivation layer and above said third portion of said connecting portion; and

a pixel electrode, located on said passivation layer, said pixel electrode electrically connecting said switching device and said coupling portion of said conducting layer through said contact window.

Claim 8. A method of fabricating a pixel structure, comprising

sequentially forming a gate electrode a gate line and a common line on a substrate, wherein the gate line is electrically connected to said gate electrode;

.....

forming a data line and a conducting layer on said gate insulating layer and forming a source electrode and a drain electrode on said channel layer, said data line being electrically connected to said source electrode, said conducting layer including a coupling portion and a connecting portion, said coupling portion being formed above said common line, said connecting portion connecting said coupling portion and said drain electrode, wherein **said connecting portion comprises a multi-channel portion and said multi-channel portion possesses a plurality of channels**;

forming a passivation layer above said substrate covering said data line, said conducting layer and said thin film transistor;

forming a contact window in said passivation layer exposing said multi-channel portion of said connecting portion; and

forming a pixel electrode on said passivation layer, said pixel electrode being electrically connected to said conducting layer through said contact window.

(***Emphasis added***) Applicants submit that claims 1 and 8 patently define over the cited arts for at least the reason that the cited art fails to disclose at least the features emphasized above.

In the present invention, the connecting portion 240 of the conducting layer 250 further comprises a multi-channel portion 224 having several channels(as shown in Fig. 4 of the present invention). Therefore, the contact window in the passivation layer and the planarization layer is located above the multi-channel portion 224 and exposes at least one of the channel of the multi-channel portion. Through the exposed channel, the pixel electrode formed over the substrate is electrically connected to the drain electrode of the thin film transistor 230 since the connecting portion 240 is connected to the drain electrode of the thin film transistor (TFT) 230.

However, in the cited art, Sakamoto et al. fails to teach or suggest that the drain electrode extended portion deemed as the conducting layer by the Examiner possesses a multi-channel structure located between the TFT and the capacitor. Furthermore, Sakamoto et al. also fail to mention or suggest that the contact window in the passivation film 10 and the irregular film 11 is located above the multi-channel structure (portion) of the conducting layer and exposes at least one of the channels. Moreover, Sakamoto et al. silence about the multi-channel portion of the conducting layer so that it is understood that there is no motivation for people skilled in the art to further modified Sakamoto's application by adding the design of the multi-channel structure/portion to the drain electrode extended portion.

For at least the above reasons that Sakamoto et al. fail to teach or suggest each element in the claims, Applicants respectfully assert that claims 1 and 8 patentably define over Sakamoto et al. Reconsideration and withdrawal of this rejection are respectively requested. Since claims 5-7 are dependent claims which further define the invention recited in claim 1, Applicants respectfully assert that these claims also are in condition for allowance. Thus, reconsideration and withdrawal of this rejection are respectively

requested.

The Office Action also rejected claims 2-4 and 9-14 under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al. in view of Matsueda (U.S. 5,173,792). The Office Action further asserted that " Sakamoto et al. lack disclosure of the connecting portion of conducting layer is a multi-channel structure.....Matsueda discloses the connecting portion of conducting layer is a multi-channel structure... ".

However, Applicants respectfully disagree with this indication. With regard to Sakamoto, Applicants respectfully submit that these claims patently define over the prior art for at least the same reasons as discussed above for the 102 rejection. Other than the reasons mentioned above for the 102 rejection, in the cited art, Sakamoto silence about that the drain electrode extended portion can further include a multi-channel portion and the contact window is located above the multi-channel portion and exposes at least one of the channels. Hence, people skilled in the art will not image to modify Sakamoto's application by adding the design of the multi-channel portion to the drain electrode extended portion. That is, there is **no motivation** founded in Sakamoto's application for using the multi-channel structure in the connection between the pixel electrode and the TFT disclosed by Sakamoto et al.

Furthermore, the Examiner asserted that the combination of the three portions (170A, 170B and 170C) of the capacitor 170, the cutoff position 151, 152 and 153 and contact hole 165 is physically and functionally equal to the connecting portion of the conducting layer of the present invention. Applicants respectfully disagree with this indication. As shown in Fig. 11 of the cited art, the capacitor 170 connects to the driving electrode 141 through a single contact hole 165 and the drains 144 and 174 of the TFTs

140A and 140B are connected to the driving electrode 141 through the contact holes 162 and 163 respectively (col. 15, lines 7-31). However, the three portions 170A, 170B and 170C deemed as the first portion of the connecting portion of the present invention by the Examiner belong to the capacitors 170 and the positions 151, 152 and 153 deemed as the channels of the present invention by the Examiner are only the cutoff positions emphasized by Matsueda (col. 15, lines 62-68). Physically, the portions 170A, 170B and 170C with the positions 151, 152 and 153 are not at the same plane as the contact hole 165 so that it is not proper to address that the portions 170A, 170B and 170C with the positions 151, 152 and 153 and the contact hole 165 are **all the portions of a conducting layer**. Further, Matsueda fails to teach or suggest to extending the joint portion of the portions 170A, 170B and 170C to directly connect to the drains 144 and 174 without assisting by the contact hole. Although Matsueda provides the capacitors 170 having the portions 170A, 170B and 170C with the positions 151, 152 and 153, Applicants respectfully submit that the combination of the portions 170A, 170B and 170C with the positions 151, 152 and 153 and the contact hole 165 is physically and functionally different from the connecting portion of the conducting layer claimed by the present invention.

Therefore, even though people skilled in the art did modified Sakamoto by referring to Matsueda., the combination result would be still different from what disclosed by the present invention and would not possess the advantage the same as what mentioned by the present invention. Hence, Applicants respectfully submit that Sakamoto et al. in view of Matsueda fails to render claims 1, 4-8 and 10-14 unpatentable. Thus, reconsideration and withdrawal of this rejection are respectively requested.

For at least the foregoing reasons, Applicants respectfully submit that independent

claims 1 and 8 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 4-7 and 10-14 patently define over the prior art as well.

Newly Added Claims

Applicants have added claims 15-20 for further limiting the present invention by introducing a blocking layer located between the substrate and the gate insulating layer below the connecting portion of the conducting layer, exposed by the contact window. No new matter is introduced to the newly added claims. As stated, claim 15 recites:

> Claim 15. (new) A pixel structure, comprising:
> a gate line located on a substrate;
> a common line located on the substrate for a bottom electrode of a pixel storage capacitor;
> a blocking layer located on the substrate between the gate line and the common line;
> a gate insulating layer located over the substrate;
> a data line located on the gate insulating layer;
> a switching device located on the substrate, wherein the switching device is electrically connected to the gate line and the data line;
> a conducting layer located on the gate insulating layer, wherein the conducting layer includes a coupling portion and a connecting portion, the coupling portion is located above the common line for a top electrode of the pixel storage capacitor and the connecting portion is connected to the coupling portion and the switching device and is located above the blocking layer;
> a passivation layer covering the data line, the switching device, and the conducting layer;
> **a contact window disposed in the passivation layer and the gate insulating layer** above the connecting portion, wherein **the contact window exposes a portion of the blocking layer and a portion of the connecting portion over the exposed blocking layer**; and
> a pixel electrode located on the passivation layer, wherein the pixel electrode is electrically connected the switching device to the coupling portion of the conducting layer through the portion of the connecting portion exposed by the contact window and **the pixel electrode is in contact with the portion of the blocking layer exposed by the contact**

window.

(*Emphasis added*) Applicants submit that claim 15 patently defines over the cited arts for at least the reason that the cited art fails to disclose at least the features emphasized above.

More specifically, in the present invention, the contact window penetrates 228 through the passivaton layer 211 and the gate insulating layer 205 to expose a portion of the blocking layer 222 (Fig. 3). In addition, the pixel electrode 212 is directly in contact with the portion of the blocking layer 222 exposed by the contact window 228.

However, none of Sakamoto and Matsueda teaches or suggests the existence of the blocking layer. Further, there is no evidence founded in both Sakamoto's application and Matsueda's application to support that the contact window penetrates through the passivation layer and the gate insulating layer to expose a portion of the blocking layer and a portion of the connecting portion over the exposed blocking layer. Therefore, even though people skilled in the art did modified Sakamoto by referring to Matsueda., the combination result would be still different from what disclosed by the present invention and would not possess the advantage the same as what mentioned by the present invention. Hence, Applicants respectfully submit that claim 15 is in condition for allowance.

Since claims 16-20 are dependent claims which further define the invention recited in claim 15, Applicants respectfully assert that these claims also are in condition for allowance according to the same reasons as discussed above.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1, 4-8 and 10-20 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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In The Drawings:

Please substitute the attached clean drawings of Figs. 2-4 for the pending drawings of Figs. 2-4. The amended portion is the deletion of "PRIOR ART".